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Nanostructure band engineering of gadolinium oxide nanocrystal memory by CF_4 plasma treatment

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Nanostructure band engineering accomplished by CF_4 plasma treatment on Gd_2O_3 nanocrystal memory was investigated. Under the CF_4 plasma treatment, the fluorine was incorporated into the Gd_2O_3 film and resulted in the modification of energy-band. A physical model was proposed to explain the relationship between the built-in electric field in Gd_2O_3 nanostructure and the improved program/erase (P/E) efficiency and data retention characteristics. The memory window of the Gd_2O_3–NC memory with CF_4 plasma treatment and postplasma annealing was increased to 3.4 V after 10^4 P/E cycling. It is demonstrated that the Gd_2O_3–NC memory with nanostructure band engineering is promising for future nonvolatile memory application. © *2010 American Institute of Physics*. [doi:10.1063/1.3462929]

During the last several decades, flash memory market has grown rapidly due to the development of portable electronic products. To solve the scaling down issue of the floating gate flash memory, the discrete charge-storage node memories have been attractive for the thinner tunneling oxide without sacrificing the retention characteristics.[1–4] Of all the discrete storage node memories, isolated Si and Ge nanocrystals (NC) have been investigated because of the simple fabrication process and high charge-storage density.[2–4] In order to achieve faster program/erase (P/E) characteristics, metal NC memories like Au, Ni, and Ru were presented to engineer the depth of the potential well as the charge storage nodes.[5–8] Compared with the semiconductor counterparts, metal NC exhibits large density of states around Fermi level, a wider range of available work function, and higher immunity against the perturbation due to carrier confinement.

Recently, the metal-oxide NC memories such as HfO_2–NC embedded in SiO_2-rich matrix have been proposed, and present good memory window and data retention.[9,10] Nevertheless, the cosputtering process faces uncertainly material properties after high temperature annealing.[11] Gadolinium oxide (Gd_2O_3), the rare-earth sesquioxides (R_2O_3), has been reported to be candidates as NC memories.[12] The crystallized Gd_2O_3–NC dots with low energy band-gap (5.0–5.4 eV) surrounded by the high energy band-gap of amorphous Gd_2O_3 dielectrics (6.3–6.4 eV) to perform the energy band offset is responsible for the charge storage.[13,14] Unfortunately, the memory characteristics of the Gd_2O_3–NC memories were still not good enough. In this work, the CF_4 plasma treatment on Gd_2O_3–NC film was studied to improve the P/E efficiency and data retention characteristics. The nanostructure band engineering of Gd_2O_3–NC memories with CF_4 plasma treatment was demonstrated and can be used in future nonvolatile memory application (NVMs).

The Gd_2O_3–NC memory devices were fabricated on n-type (100) silicon wafers. After the standard RCA (Radio Corporation of America) wafer cleaning process, a 3 nm tunnel oxide was thermally grown by horizontal furnace. Then, a 13 nm gadolinium oxide was deposited by sputtering with a pure gadolinium (99.9% pure) target in oxygen (O_2) and argon (Ar) mixture ambience at room temperature. The proportion of oxygen and argon ambient flow rate is 1:7 for amorphous Gd_2O_3 formation. After the dielectric films had been formed, the samples were rapid thermal annealed at 900 °C for 30 s in N_2 ambient to form the Gd_2O_3 NC and denoted as sample A. Then the 50 W CF_4 plasma was treated on the Gd_2O_3 films for 1 min and postplasma annealed (PPA) at 700 °C for 30 s. The sample with CF_4 plasma was denoted as sample C and following with PPA was denoted as sample D. To confirm the memory improvement by CF_4 plasma, the sample without CF_4 plasma and annealed at 700 °C was fabricated and denoted as sample B. After that, an 8 nm SiO_2 was deposited by plasma-enhanced chemical-vapor deposition (PECVD) to be the blocking oxide. A 300 nm Al film was deposited by thermal coater, and a gate was defined lithographically and etched. The capacitance-voltage (C–V) hysteresis was measured by HP4285 precision LCR meter and the P/E characteristics were measured by HP4156C to supply the gate pulse.

Figure 1(a) shows the F 1*s* x-ray photoelectron spectroscopy (XPS) depth profile analysis of the Gd_2O_3–NC memories with CF_4 plasma treatment. A take-off angle (TOA) of 90° was used to measure the XPS spectra. The maximum fluorine peak intensity was observed at the Gd_2O_3 film surface and decreased with increasing film depth, indicating that the fluorine was incorporated into the Gd_2O_3 film but decreased from surface to bulk. Figure 1(b) shows the Gd 4*d* XPS spectra of the Gd_2O_3 film with and without CF_4 plasma treatment. The ^9D peak of the sample without CF_4 plasma treatment was about 143.7 eV, which can be identified as the stoichiometric Gd_2O_3.[15] After the CF_4 plasma treatment, the binding energy was shifted, meaning that F was bonded with Gd. The high-resolution transmission electron microscopy (HRTEM) images of the samples with and without PPA (sample C and D) are revealed in inset of Fig. 1(a) and 1(b), respectively. The diameter of Gd_2O_3–NC for Sample C was 5–7 nm while increased to about 8–10 nm for sample D. It is reported that the fluorine atoms in dielectric film will result in band-gap expansion due to the high electronegativity of fluorine (the relative value is 4.0).[16,17] There-

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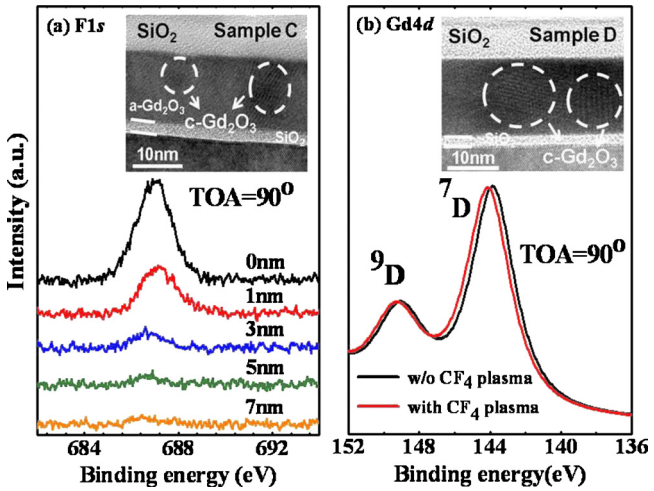

FIG. 1. (Color online) (a) The F 1*s* XPS depth profile of the Gd_2O_3–NC memory with CF_4 plasma treatment and analyzed from the Gd_2O_3 film surface. (b) The Gd 4*d* XPS analysis of the Gd_2O_3–NC memories with and without CF_4 plasma treatment. The HRTEM images of Gd_2O_3–NC memories are shown in the inset.

fore, the Gd_2O_3–NC memories with CF_4 plasma treatment presents a gradual nanostructure energy band diagram, as revealed in Fig. 2. The built-in electric fields in Gd_2O_3 film are denoted as E1 and E2 in amorphous Gd_2O_3 and Gd_2O_3–NC, respectively. Since the maximum intensity of fluorine was observed at the surface, the built-in electrical-field in amorphous Gd_2O_3 is larger than that in Gd_2O_3–NC, i.e., E1 is larger than E2.

Figure 3 demonstrates the P/E characteristics of the Gd_2O_3–NC memories. The samples were programmed at gate voltage for 12 V and erased at −13 V. The corresponding programmed (12 V for 1 ms) and erased (−13 V for 1 s) C–V curves are shown in inset figure. The program speed of the samples with CF_4 plasma was significantly improved and 2 V flat-band shift can be easily achieved at 12 V for 1 ms pulse width. This is owing to the built-in electric field in amorphous Gd_2O_3 (E1) to prevent the electrons from tunneling to the gate when applying positive gate bias. On the other hand, the faster erase speed of the sample with CF_4 plasma was also obtained because the built-in electric field in Gd_2O_3–NC (E2) will enhance electrons tunneling back to silicon substrate when applying negative gate bias, as revealed in inset band diagrams of Fig. 3. It is compulsory to notice that the erase saturation of the sample with only CF_4 plasma (sample C) was observed. This can be ascribed to some defects generated by plasma damage. After the PPA process, the defects can be eliminated and the erase characteristics can be improved.

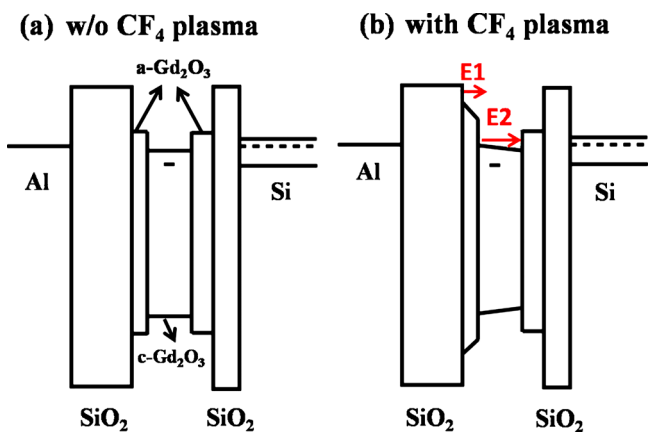

FIG. 2. (Color online) Energy band diagrams of the Gd_2O_3–NC memories (a) without and (b) with CF_4 plasma treatment, which is speculated from the fluorine XPS analysis.

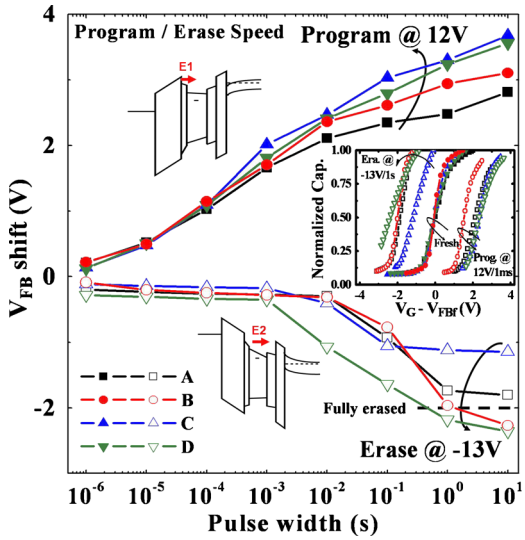

FIG. 3. (Color online) P/E speed of the Gd_2O_3–NC memories with CF_4 plasma treatment and postplasma annealing (PPA). The program and erase voltages are 12 V and −13 V, respectively. The C–V curves measured at 12 V/1 ms programming and −1 3 V/1 s erasing are shown in the inset. All the C–V curves of *x*-axis are normalized by subtracting V_{FBf}, the flat-band voltage of the fresh sample. The improved P/E characteristics by CF_4 plasma treatment can be explained by built-in E1 and E2, respectively, as shown in the inset band diagrams.

Figure 4 presents the retention characteristics of the Gd_2O_3–NC memories at room temperature. According to She's research, electrons in the storage nodes with higher energy level will collide with barrier and tunnel to the gate and substrate rapidly.[18] It can be fitted as line-1 of the retention curves. In addition, electrons in the trap states will be excited to the conduction band then tunnel to gate and substrate slowly, as displayed in the band diagrams in inset of Fig. 4, which can be fitted as line-2. The charge loss rate of

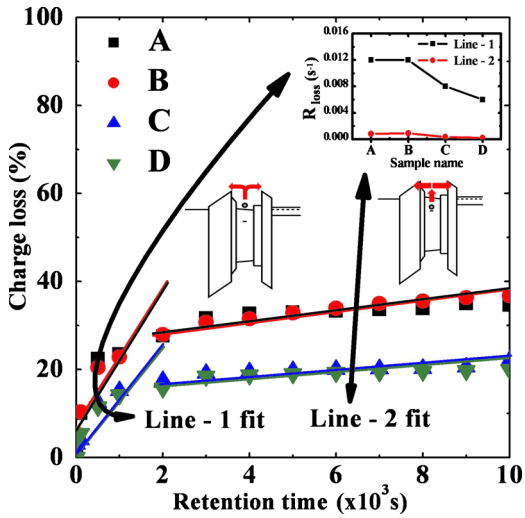

FIG. 4. (Color online) Charge retention characteristics of Gd_2O_3–NC memories with CF_4 plasma treatment and PPA at room temperature. The charge loss rate was fitted by two straight lines and shown in the inset.

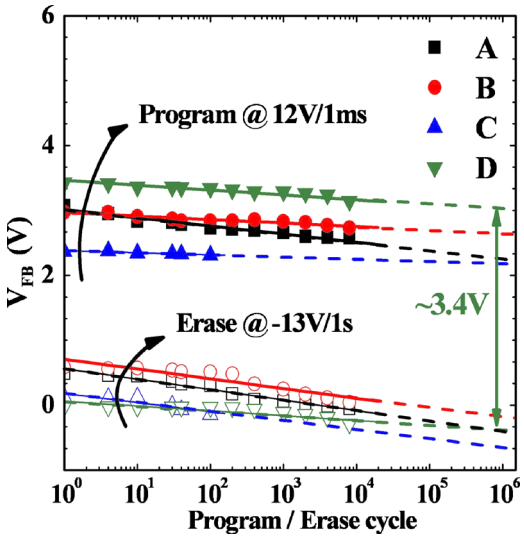

FIG. 5. (Color online) Endurance characteristics of Gd_2O_3–NC memories with CF_4 plasma treatment and PPA. The samples were programmed at 12 V for 1 ms and erased at −13 V for 1 s. Early cycling failure was observed for sample C due to the plasma damage. Sample D can sustain the memory window for over 3.4 V after 10^4 P/E cycling.

these samples was extracted and shown in the inset figure. The main difference of charge loss rate between the samples with and without CF_4 plasma treatment was resulted from the surface defect passivation by F ions and line-1 slope reduction caused by E1 to prevent high energy electrons tunneling to gate electrode. Figure 5 illustrates the endurance characteristics of the Gd_2O_3–NC memories. All the samples were programmed at 12 V for 1 ms and erased at −13 V for 1 s. We can observe that the sample with CF_4 plasma treatment and PPA can sustain the memory window for over 3.4 V after 10^4 P/E cycling. It is obligatory to mention that the early cycling failure ($<10^2$ P/E) cycling is observed for the sample with only CF_4 plasma treatment. Some defects generated by plasma damage are responsible for this.

In summary, the CF_4 plasma treatment on Gd_2O_3–NC memory was investigated to improve the P/E efficiency and data retention characteristics. The built-in electric field in Gd_2O_3 nanostructure caused by suitable fluorine incorporation will lead to the characteristics improvement. With the postplasma annealing process, the endurance characteristic was improved because of the elimination of plasma induced defects. This nanostructure band engineering technique is suitable for the future NVM use.

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