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Natural radioactivity consideration for high-κ dielectrics and metal gates choice in nanoelectronic devices

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Abstract
In order to face downscaling, new chemical elements are used and suggested for the semiconductor industry. However, some of these elements have natural radioactive isotopes, which may cause reliability issues in nanoelectronic devices by triggering soft errors. In this paper, we focus on high-κ dielectric materials and metal gates. We show that besides physical, chemical and mechanical properties of high-κ dielectrics and metal gates, natural radioactivity is also a crucial property to be considered in order to select suitable materials. Using samarium in gate oxides and platinum in electrodes turns out to be a crucial issue for ground level applications.

1. Introduction

Alpha particles are the major reliability issues in electronic devices causing soft errors at ground level [1]. They are emitted from natural disintegrations of radioactive nuclei called alpha emitters. Once emitted, alpha particles lose their energy by ionizing atoms of the medium in which they travel, resulting in the generation of charges, which are then collected by sensitive nodes. The collected charge may induce a soft error by changing a bit from state '1' to state '0' or vice versa [2]. Sources of soft errors induced by alpha particles are classified into two categories. The first source corresponds to common impurities (^{238}U, ^{232}Th and their relative daughters) that are naturally present in refined materials or incorporated into devices during their processing (e.g. residual left behind after etching with acid solutions). On the other hand, the second source corresponds to elements used in devices, naturally containing an amount of isotopes emitting alpha particles. These elements are introduced into the semiconductor industry in order to face the scaling of electronic devices ignoring sometimes their ability to emit alpha particles, (e.g. HfO_2 as a high-κ dielectric containing ^{174}Hf, which is a natural alpha emitting isotope (see table 1). This paper focuses on materials used and suggested for present and future nodes, containing alpha emitting isotopes. We evaluated the materials' contribution to soft error rate (SER) in order to evaluate their risk.

Table 1. List of radioactive isotopes contained in new elements used or suggested for the semiconductor industry [3].

Alpha emitter isotopes	Half-life (years)	Natural abundance (%)
^{174}Hf	2.0×10^{15}	0.162
^{152}Gd	1.08×10^{14}	0.20
^{144}Nd	2.29×10^{15}	23.8
^{148}Sm	7.0×10^{15}	11.3
^{147}Sm	1.06×10^{11}	15.0
^{190}Pt	6.5×10^{11}	0.01

2. New chemical elements for gate oxides and metal electrodes

Scaling of gate oxides made it possible that recent technology nodes have an oxide thickness around 10 Å. At this range, quantum tunnelling leads to unacceptable leakage current and unexpected values of key parameters affecting device operations. Thus, it appears likely that dielectrics other than SiO_2 are required for new complementary metal–oxide–semiconductor (CMOS) technologies. Solutions to this problem suggest employing high-κ materials for gate oxides [4]. High-κ insulators are materials with higher permittivity, which means they are sufficiently thicker preventing quantum tunnelling. For example, hafnium based oxides have attracted considerable attention in the last decade. As a result, Intel

integrated these oxides in its 45 nm MOS devices [5]. In spite of the approval, hafnium based gate oxides exhibit disadvantages in terms of thermodynamical stability [6–8]. Hence, investigations on attractive high-κ dielectrics suggested rare earth based oxides as future gate dielectrics [9–19]. Among these potential rare earth based gate dielectrics, Gd_2O_3 [12–14], $GdScO_3$ [15–17], $SmScO_3$ [18] and Nd_2O_3 [19] have been suggested as favourite candidates for future MOS technologies. Moreover, traditional poly-silicon gate electrodes do not satisfy the desired requirements because of the poly-silicon depletion effect (boron penetration in Si) [4]. To overcome this problem, fully silicided (FUSI) and fully germinide (FUGE) metal electrodes have been developed due to their CMOS compatibility [20]. Alloys of nickel and platinum (Ni/Pt) [20, 22], PtSi [23] and Pt_3Ge_2 [24] are proposed as gate electrodes for P-metal–oxide–semiconductor field effect transistors (P-MOSFETs). On the other hand, by alloying nickel and gadolinium, Ni(70)Gd(30) has been proposed as a metal electrode for N-MOSFETs [25]. These propositions for both gate oxides and metal electrodes rely only on physical and chemical properties as well as process compatibility, but the radioactivity aspect of the new chemical elements has not been included.

3. Alpha particle induced SER calculation

Gadolinium (Gd), samarium (Sm), neodymium (Nd) and platinum (Pt) have natural alpha emitter isotopes (see table 1). If introduced in devices, they may induce soft errors. A 32 nm half-pitch gate stack of a high performance logic technology is considered here in order to evaluate the SER of these materials. It has a gate oxide that has an equivalent oxide thickness (EOT) of 9 Å EOT. The volume of the gate oxide is 18 nm × 90 nm × 9 Å (EOT). The volume of the metal electrode is 18 nm × 90 nm × 26 nm. The dimensions of the volumes are taken from ITRS [26]. The main gate dielectrics studied in this paper are HfO_2, $GdScO_3$, Gd_2O_3, $SmScO_3$, Nd_2O_3 and the main metal electrodes studied are PtSi, Pt_3Ge_2 and the alloy of (nickel/gadolinium) Ni(70)Gd(30).

All these oxides have a dielectric constant between 10 and 25. In this paper, an average dielectric constant of 20 is taken in order to estimate the order of magnitude of the gate oxide thickness. Using the following equation, the thickness of the high-κ insulator required to form a gate oxide of 9 Å EOT is 46 Å:

$$t_{ox} = t_{eq} \times \frac{k_x}{k_{SiO_2}} \text{ [12]}, \quad (1)$$

where, t_{eq}, and t_{ox} are the thicknesses of the equivalent oxide and the high-κ dielectric, respectively. k_x and k_{SiO_2} are the dielectric constants of the high-κ dielectric and SiO_2, respectively. Hence, the volume of the gate dielectric is then 7452 nm^3 and that of the metal electrode is 42 120 nm^3. By using the basic molar mass calculation, we developed the following equation which determines the number of radioactive atoms N_0 present in these volumes:

$$N_0 = \frac{\rho V}{M} \times N_A \times \frac{a}{100} \times n, \quad (2)$$

Table 2. Summary of SER of different compounds studied.

Compound	Used as	SER (FIT/Mbit)
HfO_2	Gate oxide	0.08
$GdScO_3$	Gate oxide	3.3
Gd_2O_3	Gate oxide	4.8
Nd_2O_3	Gate oxide	9.6
$SmScO_3$	Gate oxide	7.9×10^3
PtSi	P-MOSFET metal electrode	34.2
Pt_3Ge_2	P-MOSFET metal electrode	38.0
$Ni_{70}Gd_{30}$	N-MOSFET metal electrode	6.5

where ρ is the density of the compound, V and M are the volume and the molar mass, respectively, of the gate oxide or the metal electrode. N_A is the Avogadro number, a and n are the percentage of natural abundance and the number of radioactive atoms in the molecule, respectively. Using equation (2), a 32 nm half-pitch gate made by HfO_2 contains 334 atoms of ^{174}Hf, which are alpha emitters. A unit SRAM memory cell contains six MOSFETs. In this paper, we take a 6T SRAM, thus the cell is made of six gate oxides. Assuming that the entire six transistors have the same size, a 1 Mbit memory cell encloses 2.01×10^9 atoms of radioactive ^{174}Hf. The number of disintegrations involved in these radioactive atoms is obtained by using the exponential radioactive decay law:

$$N = N_0(1 - e^{-\lambda T}), \quad (3)$$

where N, N_0 and λ are the number of emitted alpha particles, the above calculated radioactive atoms and the decay constant, respectively. T is defined as 10^9 h so that the results can be directly compared with failure in time (FIT), which represents the number of failures during 1 billion hours. Thus, a 1 Mbit memory cell, made of HfO_2 gates, undergoes 0.08 disintegrations/Mbit/10^9 h. Supposing that, in the worst case, every emitted alpha particle gives rise to a soft error, a 1 Mbit SRAM memory made by HfO_2 has a failure rate of 0.08 FIT/Mbit. This evaluation is consistent according to [21]. Note that this failure rate concerns only failures caused by alpha particles emitted from the gate oxide. The value of 0.08 FIT/Mbit has to be compared with the acceptable SER. From the ITRS road map [22], the targeted SER is between 1000 and 2000 FIT/Mbit for 32 nm based SRAM memories. Consequently, a 1 Mbit SRAM memory cell has a very low SER induced by the HfO_2 gates. Therefore, Hf based gate oxides cannot be a concern for device failures induced by alpha particles. Using the same reasoning, table 2 summarizes the failure rate caused by each material containing alpha emitters. $GdScO_3$, Gd_2O_3 and Nd_2O_3 as gate oxides, in the worst case, lead to only 3.3 FIT/Mbit, 4.8 FIT/Mbit and 9.6 FIT/Mbit, respectively. In comparison with the targeted SER, we conclude that gate oxides made of gadolinium and neodymium based compounds should not be a problem (in terms of soft error induced by alpha particles), even though the latter are alpha emitters.

The case of samarium (used in $SmScO_3$) is different. The results show that a 1 Mbit SRAM memory cell using Sm based gate dielectrics can have, in the worst case, a rate of 7.9×10^3 FIT/Mbit. This high rate is explained by a high

disintegration rate in comparison with ^{147}Sm, because it has a shorter half-life than ^{148}Sm. Hence, Sm based materials may lead to an unacceptable level of SER. However, this evaluation remains in the worst case. In fact, not all disintegrations result in soft errors. In order to estimate definitely the influence on SER, a Monte Carlo based simulation would have to be performed on the device of interest.

For metal electrodes, the SER is calculated by assuming that the 6T SRAM memory is composed of two N-MOSFETs and two P-MOSFETs to store data and two N-MOSFETs access transistors. For metal electrodes composed of Ni(70)Gd(30), the SER is negligible (6.5 FIT/Mbit). This type of electrode should not be a problem in SRAMs. Metal electrodes of P-MOSFETs, PtSi and Pt_3Ge_2, give 34.2 FIT/Mbit and 38.0 FIT/Mbit, respectively. These values may appear lower than the recommendations of ITRS but they are not negligible since the metal electrodes are near the sensitive zones. The contribution of P-MOSFETs to SER is higher than the N-MOSFETs; this is due to the high disintegration rate of platinum. The N-MOSFET composed of gadolinium will result in a low alpha particle emission rate because gadolinium has a low disintegration rate. We have to note that if platinum is used in N-MOSFETs, the SER level will increase.

4. Conclusion

To summarize, we have evaluated the SER in the worst-case approach. Gd, Hf and Nd based materials do not play a major role in triggering soft errors. This is due to their high half-life resulting in a low disintegration rate. These elements may be used in gate oxides without taking account of their contributions to soft errors. The conclusion must be, however, revised, if the quantity of these atoms based materials introduced into devices is significantly increased. In the literature, samarium is suggested to be used as a gate oxide compound ($SmScO_3$) [18]. However, in the worst-case calculation, we show a very high contribution to SER. Hence, we do not recommend using this material in nanoelectronic devices. However, if its introduction into devices is essential, its contribution to SER must first be evaluated precisely (e.g. Monte Carlo method). Otherwise, samarium isotopes, in particular ^{147}Sm, must be purified from the samarium based material. Separation of samarium isotopes can be achieved by chemical means either by crown ether [27] or by an acetate/amalgam separation system [28]. Finally, as far as platinum is used, it is also a potential source of soft errors induced by alpha particles. Even if its activity is much lower than that of samarium, its contribution to soft errors must be taken into account because of its proximity with the sensitive zones.

References

[1] Autran J L, Roche P, Sauze S, Gasiot G, Munteanu D, Loaiza P, Zampaolo M and Borel J 2009 Altitude and underground real time SER characterization of CMOS 65 nm SRAM *IEEE Trans. Nucl. Sci.* **56** 2258–66

[2] May T C and Woods M H 1979 Alpha particle induced soft error in dynamic memories *IEEE Trans. Electron Devices* **26** 2–9

[3] Wrobel F, Gasiot J, Saigné F and Touboul A D 2008 Effects of atmospheric neutrons and natural contamination on advanced microelectronic memories *Appl. Phys. Lett.* **93** 064105

[4] Robert C *et al* 2005 Application of high-κ gate dielectrics and metal gate electrodes to enable silicon and non silicon logic nanotechnology *Microelectron. Eng.* **80** 1–6

[5] http://www.eetasia.com/ART_8800499271_480200_NT_4eb0cd7b.HTM

[6] Doering R and Nishi Y 2008 *Handbook of Semiconductor Manufacturing Technology* (Boca Raton, FL: CRC Press) pp 9–11

[7] Gusev E P, Narayanan V and Frank M M 2006 Advanced high-κ dielectric stacks with polySi and metal gates: recent progress and current challenges *IBM J. Res. Dev.* **50** 387–410

[8] Ramgopal V and Hiroshi I 2007 Rare earth oxides in microelectronics *Rare Earth Oxide Thin Films* (Berlin: Springer) p 345

[9] Leskela M and Ritala M 2006 Rare-earth oxide films for gate dielectrics in microelectronics *J. Alloys Compounds* **418** 27–34

[10] Leskela M and Ritala M 2003 Rare-earth oxide thin films as gate oxides in MOSFET transistors *J. Solid State Chem.* **171** 170–4

[11] Scarel G and Fanciulli M 2007 *Rare Earth Oxide Thin Films: Growth, Characterization, and Applications* (Berlin: Springer) p 1

[12] Osten H J, Laha A, Czernohorsky M, Bugiel E, Dargis R and Fissel A 2008 Introduction crystalline rare-earth oxides into Si technologies *Phys. Status Solidi* a **205** 695–707

[13] Yue S, Wei F, Wang Y, Yang Z and Du J 2009 Gd_2O_3 high-κ gate dielectrics deposited by magnetron sputtering *Symp. D, E and F MRS Int. Materials Research Conf.; J. Phys.: Conf. Ser.* **152** 012004

[14] Dimoulas A, Gusev E, McIntyre P C and Heyns M 2007 *Advanced Gate Stacks for High-Mobility Semiconductors* (Berlin: Springer) p 229

[15] Lopes J M J *et al* 2009 Amorphous ternary rare-earth gate oxides for future integration in MOSFETs *Microelectron. Eng.* **86** 1646–9

[16] Wagner M, Heeg T, Schubert J, Lenk St, Mantl S, Zhao C, Caymax M and De Gent S 2006 Gadolinium scandate thin films as an alternative gate dielectric prepared by electron beam evaporation *Appl. Phys. Lett.* **88** 172901

[17] Roeckerath M, Lopez J M J, Durgun Ozben E, Sandow C, Lenk S, Heeg T, Schubert J and Mantl S 2009 Gadolinium scandate as an alternative gate dielectric in field effect transistors on conventional and strained silicon *Appl. Phys.* A **94** 521–4

[18] Durgun Ozben E, Lopes J M J, Roeckerath M, Lenk St, Hollander B, Jia Y, Schlom D G and Schubert J 2008 $SmScO_3$ thin films as an alternative gate dielectrics *Appl. Phys. Lett.* **93** 052902

[19] Pan T M, Lee J, Shu W and Chen T T 2006 Structural and electrical properties of neodymium oxide high-κ gate dielectrics *Appl. Phys. Lett.* **89** 232908

[20] Doering R and Nishi Y 2008 *Handbook of Semiconductor Manufacturing Technology* (Boca Raton, FL: CRC Press) pp 10-40–10-45

[21] Wrobel F, Gasiot J and Saigné F 2008 Hafnium and uranium contributions to soft error rate at ground level *IEEE Trans. Nucl. Sci.* **55** 3141–5

[22] http://www.fsi-intl.com/index.php/applications-and-products/mol-strip-clean/299-stmicroelectronics-describes-zetar-system-vipr-process-in-metal-stripping-for-nickel-platinum-silicide
[23] Kadoshima M *et al* 2005 Silicon-atom induced Fermi-level pinning of fully silided platinum gates on HfO_2 dielectrics *Japan. J. Appl. Phys.* **44** 2267–72
[24] Tsuchiya Y, Koyama M, Koga J and Nishiyama A 2006 Material characterization of metal germanide gate electrodes formed by fully germanided gate process *Japan. J. Appl. Phys.* **45** 2925–32
[25] Lee B, Biswas N, Novak S R and Misra V 2007 Characteristics of Ni/Gd FUSI for NMOS gate electrode applications *IEEE Electron. Device Lett.* **28** 555–7
[26] http://www.itrs.net/Links/2008ITRS/Home2008.htm
[27] Fujii T, Nishizawa K, Yamamoto T, Inagawa J, Gunji K and Watanabe K 1997 Separation of gadolinium and samarium isotopes by crown ether *Technology Reports 45* Osaka University pp 119–26
[28] Dembinski W 2001 Isotopes effects of samarium and ytterbium in the acetate/amalgam separation system *J. Radio. Anal. Nucl. Chem.* **250** 423–8